CLAIMS

What is claimed is:

1. An electrical circuit comprises:

(a)a plurality of voltage controlled capacitors with different capacitance values in different ranges of bias voltages;

(b)a plurality of input signals connected to said capacitors in (a);

(c)an output signal connected to a plurality of capacitors in (a); and

(d)a sensing circuit connected to the output signal in (c), and the output of said sensing circuit in (d) is determined by the coupling voltages between said input signals in (b) and said output signal in (c) through said capacitors in (a).

2. The electrical circuit in claim 1 is a programmable logic array (PLA).

3. The electrical circuit in claim 1 is a memory device.

4. The electrical circuit in claim 1 is an optical sensor.

5. The electrical circuit in claim 1 shares the same area with other active devices to form a 3 dimensional device.

6. The electrical circuit in claim 1 uses metal-oxide-semiconductor (MOS) devices as voltage controlled capacitors, said MOS devices comprising:

(a)a semiconductor substrate;

(b)a thin film insulator layer deposited on said semiconductor substrate in (a); and

(c)a conductor layer deposited on said thin film insulator layer in (b).

7. The electrical circuit in claim 6 is a programmable logic array (PLA).

8. The electrical circuit in claim 6 is an electrical optical sensor.

9. The electrical circuit in claim 6 shares the same area with other active devices to form a 3 dimensional device.

10. The MOS device in claim 6 has p-type semiconductor substrate.

11. The MOS device in claim 6 has n-type semiconductor substrate.

12. The electrical circuit in claim 1 uses floating gate devices as voltage controlled capacitors, said floating gate device comprising:

(a)a semiconductor substrate;

(b)a thin film insulator layer deposited on said semiconductor substrate in (a);

(c)a floating gate deposited on said thin film insulator layer in (b);

(d)a thin film insulator layer deposited on said floating gate in (c); and

(e)a conductor layer deposited on said thin film insulator layer in (d).

13. The electrical circuit in claim 12 is a field programmable logic (FPG) circuit.

14. The electrical circuit in claim 12 is a memory device.

15. The electrical circuit in claim 12 shares the same area with other active devices to form a 3 dimensional device.

16. The floating gate device in claim 12 has p-type semiconductor substrate.

17. The floating gate device in claim 12 has n-type semiconductor substrate.

18. The floating gate device in claim 12 has source and drain regions to form a floating gate transistor.

19. The floating gate transistor in claim 18 is connected to nearby floating gate transistors in series NAND configuration.

20. The floating gate transistor in claim 18 is connected to nearby floating gate transistors in parallel NOR configuration.

21. An electrical device comprises a plurality of floating gate transistors where the gates of said floating gate transistors are connected to the same input signal (word line), and the source and drain terminals are connected in series for said floating gate transistors connected to the same word line.

22. A memory device in claim 21 where nearby floating gate transistors that are connected to different word lines share the source and drain connections in parallel configuration.

23. A floating gate array comprises floating gate devices manufactured on both n-type and p-type substrates.

24. The substrates for the n-type floating gate devices in claim 23 are used to isolate the substrates for the p-type floating gate devices.

25. The substrates for the p-type floating gate devices in claim 23 are used to isolate the substrates for the n-type floating gate devices.